REMARKS

Claims 1, 2, 4 – 18, and 20 - 23 remain in the present application.

112 Rejections

The present Office Action indicates that Claims 15 – 18 and 20-23 remain rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regard as the invention.

Applicant has amended Claim 15. With regards to a configurable phase generator, Applicant respectfully reasserts that one of ordinary skill in the art would understand Claims 15 to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In addition to particularly pointing out and distinctly claim the subject matter which Applicant regards as the invention on its face, the Applicant respectfully asserts the Claim can be interpreted in light of the specification and respectfully directs the Examiner to element 430 as one exemplary implementation of a configurable phase generator.

Applicant has amended Claim 20 to read in part "a feedback line" and "a control signal".

Applicant has amended Claim 16 to read in part "a signal received via a first feedback line from said configurable phase generator".

With respect to Claim 18, Applicant respectfully reasserts that the rejections of the claims reflect an improper application of 35 U.S.C. 112, second paragraph. Applicant respectfully reasserts that claims are not required to specify every element required for enablement if one of ordinary skill in the art would understand. Applicant respectfully reasserts that one of ordinary skill in the art would understand Claims 18 to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In addition to particularly pointing out and distinctly claim the subject matter which Applicant regards as the invention on its face, the Applicant respectfully asserts the Claim can be interpreted in light of the specification and respectfully directs the Examiner to Figure 5 as one exemplary implementation how delay elements comprise an input of a respective multiplexer for selectively coupling a plurality of delay elements with a first feedback line.

102 Rejections

Claims 10, 12 - 17, and 20 - 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Zarate et al. (US 6,937,077). Applicant has reviewed the Zarate et al. reference and, for the following rationale, Applicant respectfully asserts that the present invention is not anticipated nor rendered obvious by the Zarate et al. reference.

Applicant respectfully asserts that the Zarate et al. reference is not directed to the present invention as recited in Claims 10, 12 – 17 and 20-23. Specifically the present invention, as set forth in independent Claim 10 recites in part:

> ... generating a signal by a phase detector to cause said phase generator to operate in a phase locked loop mode; ... .

To the extent the Zarate et al. reference may show a phase detector 204 [Figure 2] forwarding a control signal 288 indicating the DLL path is locked [Figure 2, Col 8 lines 37 – 40] , Applicant respectfully reasserts the Zarate et al. reference does not teach generating a signal by a phase detector (emphasis added) to cause said phase generator (emphasis added)to operate in a phase locked loop mode. To the extent the Zarate et al. reference may mention a signal selector 202 is

responsible for switching between DLL and PLL modes and does so based upon external clock signal 220 and feedback signal 222 experiencing jitter [Col 7, lines 29 – 39, Col 8 lines 10 – 13 and Col 8 lines 25 – 27], Applicant respectfully reasserts the Zarate et al. reference does not teach generating a signal by a phase detector (emphasis added) to cause said phase generator to operate in a phase locked loop mode.

The present Office Action alleges the delay line 206 of the Zarate et al. reference is a phase generator. To the extent the Zarate et al. reference may mention phase detector 204 indicates to a signal selector 202 (emphasis added) via control line 228, that a PLL to DLL mode switch should occur [Col.9 lines 33 – 35], Applicant respectfully asserts the Zarate et al. reference does not teach phase detector 204 generates a signal to cause the alleged phase generator "delay line 206" to operate in a phase locked loop mode. Applicant respectfully asserts that to the extent the Zarate et al. reference may mention the phase detector 204 indicates to a signal selector 202 (emphasis added), it does not teach the phase detector 204 indicates to delay line 204. Applicant respectfully asserts the control line 228 of Zarate et al. goes to signal selector 202 and not delay line 206.

Applicant respectfully asserts Claims 10 - 14 are allowable as depending from allowable independent Claim 10.

Similarly, with respect to Claim 15, Applicant respectfully asserts the Zarate et al. reference does not teach the recited present invention. Specifically the present invention, as set forth in independent Claim 15 recites in part:

> ...a phase detector for generating a control signal to control configuration changes of said configurable phase generator... .

To the extent the Zarate et al. reference may mention a phase detector 204 indicates to a signal selector via control line 228 that a PLL to DLL mode switch should occur [Col. 9, lines 33 – 35], Applicant respectfully asserts the Zarate et al. reference does not teach a phase detector generates a control signal to control configuration changes <u>of a configurable phase generator</u> (emphasis added). To the extent the Zarate et al. reference may mention a signal selector 202 is responsible for switching between DLL and PLL [Col 7, lines 29 – 39, Col 8 lines 10 – 13 and Col 8 lines 25 – 27], Applicant respectfully asserts the Zarate et al. reference does not teach a configurable phase generator. Again, the present Office Action alleges the delay line 206 of the Zarate et al. reference is a phase generator. Applicant respectfully asserts the control line 228 of Zarate et al. goes to signal selector 202 and not delay line 206.

Applicant respectfully asserts Claims 16 – 18 and 20 – 23 are allowable as depending from allowable independent Claim 15.

103 Rejections

The present Office Action indicates Claims11 and 18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Zarate et al. in view of Paakinson et al. (D404227314A). Applicant was not able to locate a Paakinson et al. (D404227314A) reference. To the extent the current Office Action is referring to Paakinson et al (JP404227314A) partially translated and attached to a previous Office Action, Applicant respectfully asserts that the present invention is neither shown nor suggested by the Zarate et al. nor the Paakinson et al. references, alone or together. In addition, Applicant respectfully asserts a person of ordinary skill in the art would not find a motivation or suggestion to combine the teachings of the Zarate et al. and the Paakinson et al. references to teach the present claimed invention.

Applicant respectfully asserts that the present invention is neither shown nor suggested by the Zarate et al. reference for the reasons

indicated above. The present Office Action acknowledges that the Zarate et al. reference fails to teach that each delay block is associated with a multiplexer.

Applicant respectfully asserts that the Paakinson et al. reference does not overcome these and other shortcomings of the Zarate et al. reference. To the extent the Paakinson et al. reference may mention the a multiplexer is formed by forming current switches in a tree which is able to control a delay time through the adjustment of an input resistor RD and the multiplexers having a function of the delay elements are connected in cascade [Abstract/ Constitution], Applicant respectfully asserts the Paakinson et al. reference does not teach coupling each set of said plurality of dynamically controlled delay blocks with the respective multiplexer wherein an output of each of said delay element is an input to said respective multiplexer. To the extent the Paakinson et al. reference may be interpreted as forming internal components of a multiplexer, Applicant respectfully asserts the Paakinson et al. reference does not teach external coupling to a multiplexer.

Allowed Subject Matter

Applicant thanks the Examiner for indicating Claims 1-2 and 4-9 are allowed.

CONCLUSION

In light of the above-listed amendments and remarks, Applicant respectfully request allowance of the remaining Claims. The examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO

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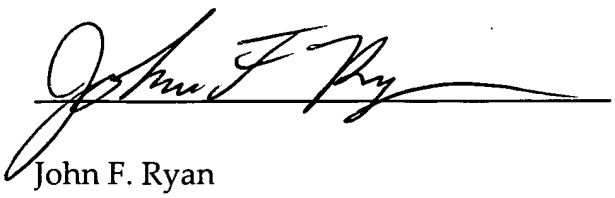

John F. Ryan
Reg. No. 47,050

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060